International Journal of Advance Scientific Research
(ISSN – 2750-1396)
VOLUME 03 ISSUE 10 Pages: 212-220
SJIF IMPACT FACTOR (2021: 5.478) (2022: 5.636) (2023: 6.741)
OCLC – 1368736135
Crossref doi Google Scholar WorldCat MENDELEY


Journal Website: http://sciencebring.com/index.php/ijasr



Research Article

# PHASE SHIFT KEYING DETECTION USING DIRECT TRANSFORM METHOD

**Submission Date:** October 14, 2023, **Accepted Date:** October 19, 2023,
**Published Date:** October 24, 2023
**Crossref doi:** https://doi.org/10.37547/ijasr-03-10-35

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## ABSTRACT

The physical interface for transmitting telemetric information (TMI) in the BITS-2T structure is represented by a physical interface for transmitting telemetric potential code (Manchester II code). The ManchesterII code is a code with redundancy, a logical one is encoded by a negative edge of the signal in the middle of a bit interval, zero by a positive edge. At the boundaries of a bit interval, the signal, if necessary, changes its value, “preparing” to display the next bit in the middle of the next bit interval.

## KEYWORDS

BITS-2T, Manchester II, Code, ADC, IC S042P.

## INTRODUCTION

The shape of the modulating voltage of the TMI signal is shown in Fig. 1. When switching the logical levels of the modulating voltage of the TMI signal, in addition to changing the carrier frequency, a short-term shift occurs phases of carrier oscillations – phase shift keying Phase shift keying serves to synchronize the TMI data stream [1,2,3]. The duration of phase shift keying is short and is about 0.2 times the period of oscillation of the carrier frequency. At carrier frequency $f_н$= **70** MHz this value will be determined as:

$$t_{ф.м.}=\frac{1}{f_н}\cdot 0.2=\frac{1}{70\cdot 10^6\ Гц}\cdot 0.2\approx 3\ ns$$

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The short duration of phase shift keying makes high-quality digitization of a TMI signal at a frequency of 70 MHz using analog-to-digital converters (ADCs) very difficult. When receiving data in streaming mode, a processing delay of several carrier cycles will inevitably lead to a failure in stream synchronization, making further software processing impossible. Therefore, to lower the carrier frequency, devices are used that detect the primary signal at its own carrier frequency, followed by modulation at the required frequency. This method has a number of disadvantages [4,5,6,7]:

- complexity of the implementation of a broadband FPS detector;
- there is no information about the initial phase at the output signal;
- lack of hot backup capability;
- the need to restart the system to recover from an error;
- absence of a local oscillator frequency control circuit.

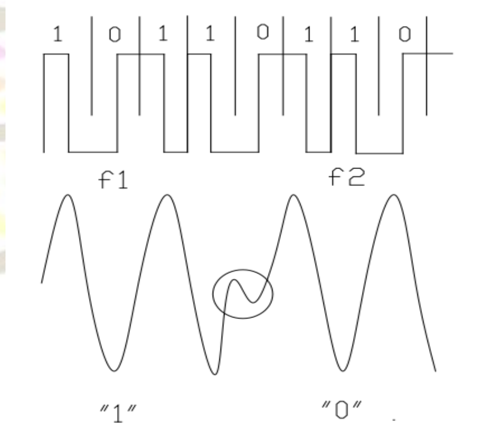


**Fig. 1. Logic levels in the Manchester-II coding system and carrier frequency, modulated by the input bit sequence.**

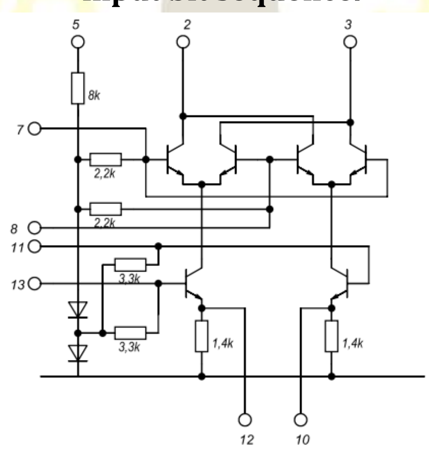


**Fig. 2. Internal circuit of IC S042P**

From the point of view of the result of information processing, this leads to an increase in the likelihood of errors [8,9] and increased system recovery time after a failure. The transition to low frequency and secondary modulation of the signal can be avoided by using a converter circuit with direct connections in the mixer [10,11,12,13].

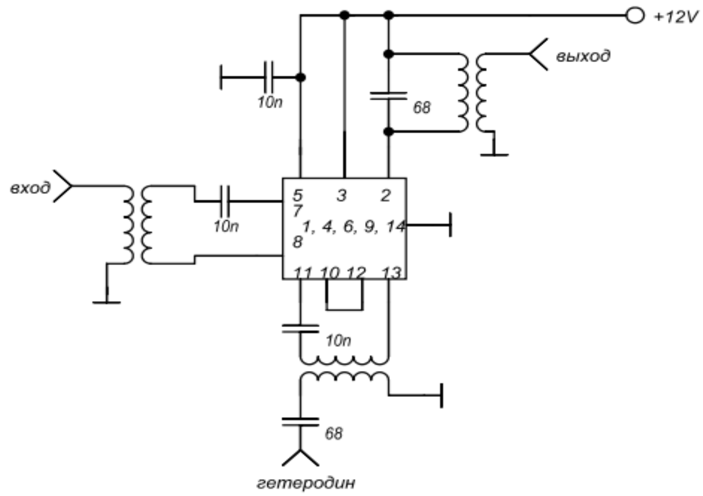


**Fig. 3. Typical connection diagram**

The absence of serial reactive elements on the path of the useful signal allows FPS signals to be processed without distortion. Mixers with direct communications are implemented in some IC models intended for radio receiving equipment. Spacecraft TMI ground processing stations use equipment similar to VertexRSI, which has an output frequency of 70 MHz, according to [14,15,16]. The S042P chip is suitable for the required frequency range. Figure 2 shows the internal circuit of S042P. From Fig. 2 it is clear that the IC contains a push-pull self-oscillator with automatic bias, an amplifier and a mixer. A typical S042P connection diagram is shown in Fig. 3. Despite the simplicity of the strapping, in the original In this case, this circuit is not suitable for processing FPM signals, due to external reactive elements in the mixer circuit and the input circuit, which do not allow the transmission of phase shift keying [17,18,19] (Fig. 3). If you exclude pass-through capacitors from the IC circuit and use an internal oscillator, you can achieve signal transmission with short-term phase shift keying. This makes it possible to process the telemetry information signal from the spacecraft. The diagram of this design is shown in Fig. 4. The wiring of each S042P link is minimal and contains only an input circuit, an output circuit connected directly to the pins of the microcircuits, a frequency shift circuit and capacitors necessary for the operation of the local oscillator integrated into the IC [20-24]. The input signal at a frequency of 70 MHz is supplied to the coupling coil L1 -of the parallel oscillatory LC circuit (hereinafter

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referred to as the circuit, since it does not contain serial ones) C2-L2. The connection between the LNA output and the L1 coil is direct and therefore does not lead to phase distortion of the input signal. L2-C2 is the only circuit tuned to the frequency of the input signal. After setting up the converter, its parameters are not are being adjusted. Coil L2 is connected directly to the input of the microcircuit (pins 1 and 11) [25-31]. C6 and L3 represent a frequency shift circuit and are tuned to frequency;

$$f_{\Gamma 1} = f_{B} + f_{\Pi 1}$$

where: f_(Г1 )– frequency of the first local oscillator, f_B– input frequency (70 MHz), f_П1– first intermediate frequency (32 MHz). Thus, the first local oscillator is tuned to the frequency:

$$f_{\Gamma 1} = 102 \text{ МГц}$$

At the output of the first link of the converter (pins 2 and 3) a parallel circuit L4-C10 is also installed, and coil L4 is tapped from the middle, this is necessary to supply power to the microcircuit. Except In addition , this solution increases the load capacity the output of the microcircuit is 1.5 times due to the fact that the oscillations at pins 2 and 3 are antiphase ( push-pull operating mode of the integrated circuit control unit ). At pins 2 and 3, an FMS signal is generated that exactly copies the input one, but with a frequency of 32 MHz (the first intermediate frequency). Through the communication coil L5 (for circuit L4-C10) the signal at the first intermediate frequency it is supplied to the input of the second converter link, designed similarly to the first. Circuit L6-C14 is tuned to 38.5 MHz. IN As a result, a signal with a carrier frequency of 6.5 MHz is generated at the output of the mixer. This signal also exactly copies the input one [32-35]. Coupling coil L8 of circuit L7-C17 is common for supplying a signal to the output connector of the converter and to the input of the UFC3-2 assembly (pin 3). The reference voltage of the APCG system is formed at pin 5 of the UPCH3-2 assembly. This voltage is supplied through resistors R6, R4, R3 to the anode of the varicap VD2. Cathode VD2 is connected through decoupling capacitors C4 and C9 to the frequency shift circuit of the first local oscillator. resistor R9 is a voltage divider, which, through R7, allows you to change the constant voltage level at the varicap terminals within small limits and thereby set the “zero” of the APCG system. This level is also adjusted once and remains constant throughout the entire operation of the converter. Data for winding units are given in Table 1. The converters are powered through resistors R5 and R10 from a common source with a constant voltage of 10.2 V. C11 and C18 are blocking capacitors. UPC3-2 is powered directly from the same source (pin 4 assembly).

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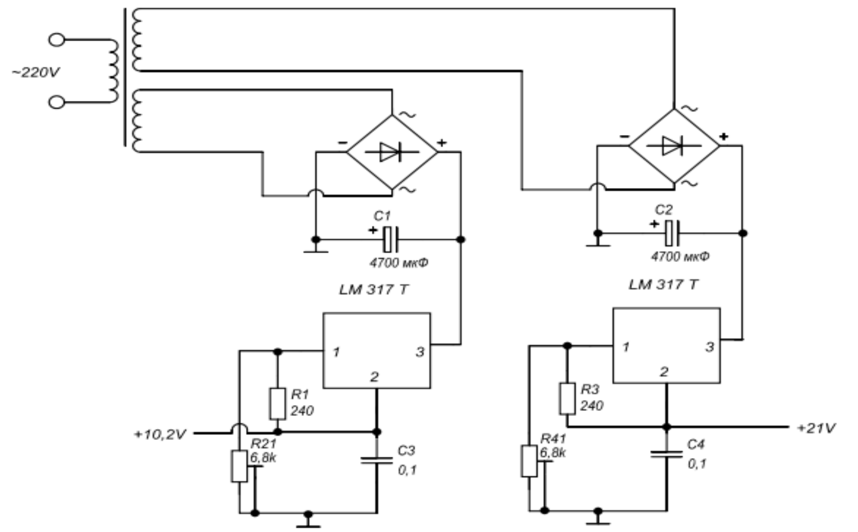


**Fig. 4. Schematic diagram of the converter power supply**

The power supply diagram is shown in Fig. 4. Two stabilized power supplies necessary for the converter to operate are implemented on the IC K142EN12A. Stabilization voltages 10.2 V and 21 V can be adjusted by rotating the potentiometer sliders, achieving optimal operating mode of the S042P IC and local oscillator frequency adjustment circuits. The operating characteristics of the implemented converter are given in Table

2. The type of TMI signal, modulated by the input bit sequence, taken from the converter output to frequency 6.5 MHz is shown in Fig. 6. Thus, the converter lowers the carrier frequency from 70 MHz to 6.5 MHz while maintaining the signal structure. Minimum duration of phase manipulation at TMI transmission in the structure of BITS-2T is:

$$t_{ф.м.}=\frac{1}{f_н}\cdot 0.2=\frac{1}{6{,}5\cdot 10^6\ Гц}\cdot 0.2\approx 3\ 1\ ns$$

Table 1. Winding unit data

| *Designation* | *L1* | *L2* | *L4* | *L5* | *L7* | *L8* | *L6* | *L3* |
|---|---|---|---|---|---|---|---|---|
| Wire diameter | 0,3 | 0,3 | 0,5 | 0,5 | 0,3 | 0,5 | 0,3 мм | 0,3 мм |
| Number of turns | 2 | 7 | 12 | 4 | 20 | 4 | 13 | 5 |
| Core material | without core | | | | ferrite | | | |
| Mandrel diameter | 6mm | | 5 mm | | 7 mm | | 6 mm | 4 mm |
| Frequency | 70MHz | | 32 MHz | | 6,5 MHz | | 38,5 MHz | 102 MHz |

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| Parameter | Meaning |
|---|---|
| input frequency | 70 MHz |
| output frequency | 6.5 MHz |
| wave impedance on the input side | 75 0m |
| output impedance | 50 0m |
| type of modulation | CFM |
| strip width not less | 29 MHz |
| self-noise level is no worse | -40 dB |
| sensitivity is no worse | 0.125 V |
| output signal amplitude not less than | 0.5 V |

The obtained value of the duration of phase shift keying allows you to process the TMI signal using ADC of the data acquisition board (for example, high-speed data acquisition board BIn25-1201) in automatic mode. In this case, the difference in the initial phases of the signals at the input and output of the converter is constant. The converter circuit contains an APCG chain, which increases the signal-to-noise ratio of the receiving system as a whole and reduces the requirements for stability of the frequency of the original signal. The UFC3-2 assembly has a low-frequency output, which allows the use of automatic transfer switching devices (ATR ) in redundant circuits. Thus, the use of a converter built according to the stated design, it makes it possible to increase the reliability of the TMI reception system and reduce the likelihood of errors.

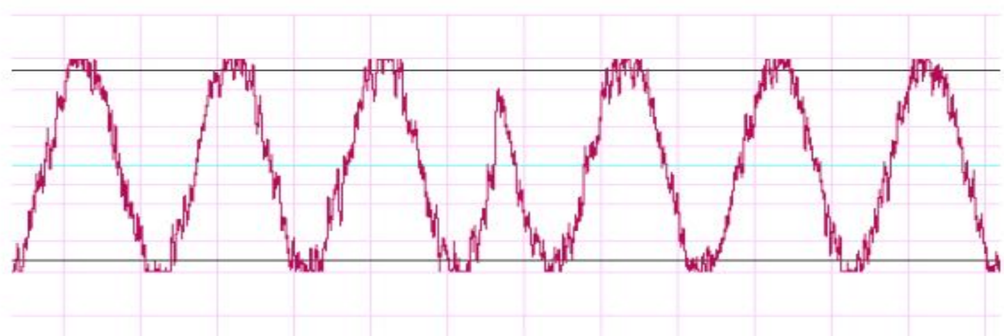

**Fig. 5. Signal, modulated by the input bit sequence at the output of the converter.**

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