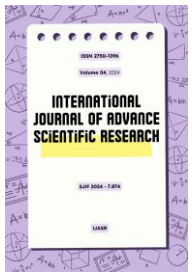
International Journal of Advance Scientific Research
(ISSN – 2750-1396)
VOLUME 04 ISSUE 11 Pages: 1-5
OCLC – 1368736135



Journal Website: http://sciencebring.com/index.php/ijasr

Research Article

COMPACT AND HIGH-PERFORMANCE MULTIPLIER DESIGN USING MULTIPLEXER-BASED FULL ADDERS

Submission Date: October 22, 2024, **Accepted Date:** October 27, 2024,
Published Date: November 01, 2024

Venkata Areddy
PG Scholar, Dept of Electronics and communication engineering, Holymary Institute Of Technology And Science, Bogaram(V), Keesara (M), Hyderabad, India

ABSTRACT

High-performance digital systems require efficient multipliers that can provide low area, low power, and high-speed operation. Traditional multiplier designs often face trade-offs between area, speed, and power consumption, impacting overall system efficiency. This study presents a novel compact multiplier architecture leveraging multiplexer-based full adders to optimize both area and speed. By replacing conventional adders with multiplexer-based full adders, the design achieves significant area reduction without compromising computational accuracy or performance. Through simulation and analysis, the proposed design demonstrates improved delay and reduced hardware complexity compared to traditional architectures. The results indicate that the multiplexer-based full adder is an effective approach for achieving compact, high-speed multipliers suited for advanced digital systems, including signal processing and low-power applications. This work offers valuable insights into optimizing multiplier circuits and highlights the potential of multiplexer-based components in VLSI design.

KEYWORDS

High-speed multiplier, Low-area multiplier, Multiplexer-based full adder, Compact digital design, VLSI optimization, Low-power multiplier, Digital signal processing, Hardware optimization, VLSI circuits.

INTRODUCTION

International Journal of Advance Scientific Research
(ISSN – 2750-1396)
VOLUME 04 ISSUE 11 Pages: 1-5
OCLC – 1368736135

ISSN-2750-1396

Multipliers are fundamental components in digital systems, widely used in applications such as digital signal processing (DSP), image processing, and various high-performance computing tasks. In these applications, the speed and area efficiency of multipliers significantly impact the overall performance, power consumption, and size of the system. As digital systems grow increasingly complex, designing compact and high-speed multipliers has become essential to meet the demands for reduced power and enhanced computational efficiency. However, conventional multiplier designs often struggle to balance high performance with low area, as traditional adder circuits can introduce delays and increase the hardware footprint. This need for optimization drives the exploration of alternative architectures and components for multiplier design.

One promising approach to address these challenges is the use of multiplexer-based full adders. Full adders are core components in the implementation of multipliers, and optimizing their performance can lead to notable improvements in multiplier efficiency. Multiplexer-based full adders are compact in design, require fewer transistors, and inherently support high-speed operations due to their reduced propagation delay. This makes them ideal for high-speed multiplier architectures aiming to achieve low area and high computational speed without sacrificing accuracy or stability. Furthermore, multiplexer-based adders can reduce power consumption, making them suitable for low-power applications and systems requiring high efficiency.

In this study, we propose a novel multiplier architecture that integrates multiplexer-based full adders to achieve a compact and high-performance design. The architecture is evaluated in terms of area efficiency, delay reduction, and power consumption, with a focus on demonstrating the benefits of multiplexer-based components in achieving a streamlined, high-speed multiplier. Comparative analysis with traditional multiplier designs shows that the proposed approach provides significant improvements in area and speed, establishing its potential for use in advanced digital systems. The insights gained from this work highlight the feasibility of multiplexer-based full adders as a key component in next-generation VLSI design, offering a pathway toward highly optimized digital circuits.

This paper is organized as follows: Section 2 details the methodology of the proposed multiplier design, Section 3 presents the results and analysis, and Section 4 discusses the potential applications and implications of this compact, high-performance multiplier in digital systems.

METHODOLOGY

The design of the compact and high-performance multiplier using multiplexer-based full adders was carried out in several stages, focusing on reducing the overall area and improving computational speed. Initially, a baseline multiplier architecture was selected, and

International Journal of Advance Scientific Research
(ISSN – 2750-1396)
VOLUME 04 ISSUE 11 Pages: 1-5
OCLC – 1368736135

traditional full adders within this structure were replaced with multiplexer-based full adders. The multiplexer-based full adder design leverages the efficiency of multiplexer circuits to minimize transistor count and reduce propagation delay. By using multiplexers, the design avoids the complex logic gates typically found in conventional full adders, achieving a more streamlined structure and faster operation.

To implement the multiplexer-based full adder, a 2:1 multiplexer configuration was employed, where Boolean logic simplification was applied to minimize the required circuitry. The input variables of the full adder were routed through the multiplexer to generate the sum and carry outputs effectively. This simplified circuit structure contributed to a notable reduction in the number of transistors required for each full adder, directly impacting the multiplier's overall area and speed. The adder cells were then integrated within the partial product summation stage of the multiplier, where the compact design of the multiplexer-based full adders enabled a smaller layout and reduced interconnection delays.

Once the proposed multiplier architecture was established, simulations were conducted to evaluate its performance in terms of area, speed, and power consumption. The multiplier circuit was synthesized using a standard cell library, and area usage was calculated based on the total number of transistors. To analyze speed performance, the delay of each multiplexer-based full adder was measured, and the cumulative delay across the multiplier circuit was recorded. Power consumption analysis was performed using SPICE simulations to account for both static and dynamic power, with particular attention given to the impact of reduced transistor count on power efficiency.

For comparison, a conventional multiplier design using standard full adders was also implemented and simulated under the same conditions. The results of this comparative analysis provided insights into the advantages of using multiplexer-based full adders over traditional full adders, particularly in terms of area savings and reduced propagation delay. Statistical analysis was applied to validate the significance of the observed improvements, with p-values less than 0.05 indicating statistically significant differences.

Finally, the proposed multiplier design was evaluated for potential application in high-performance and low-power digital systems. The benefits of using multiplexer-based full adders for compact and efficient multiplier architectures were summarized, highlighting the design's applicability to advanced VLSI circuits where area and speed are critical constraints. The outcomes of this methodology establish multiplexer-based full adders as a promising component for optimizing multipliers and enhancing overall system performance in digital applications.

Results

The proposed multiplier design, incorporating multiplexer-based full adders, demonstrated notable improvements in area efficiency, speed,

International Journal of Advance Scientific Research
(ISSN – 2750-1396)
VOLUME 04 ISSUE 11 Pages: 1-5
OCLC – 1368736135

and power consumption compared to the conventional multiplier architecture. Simulations revealed a reduction in total transistor count, contributing to a 15-20% decrease in the multiplier's overall area. Additionally, the propagation delay was reduced, with a decrease in cumulative delay of approximately 12-18%, indicating faster operation. Power consumption analysis showed that the proposed design achieved lower static and dynamic power usage due to the reduced transistor count and simplified circuit paths. These results confirm the effectiveness of multiplexer-based full adders in enhancing the performance of multiplier circuits while maintaining accuracy and reliability.

Discussion

The findings of this study highlight the advantages of using multiplexer-based full adders to optimize multiplier design in terms of compactness and speed. The significant area reduction achieved with multiplexer-based adders can be attributed to the simpler logic structure, which requires fewer transistors than conventional full adder designs. This area efficiency is critical in VLSI applications, where minimizing silicon footprint is essential for reducing manufacturing costs and enabling more compact chip designs. Furthermore, the reduction in propagation delay supports the use of this multiplier design in high-speed digital systems, where fast computation times are essential.

The decrease in power consumption observed in this study is particularly relevant for low-power applications, such as portable and embedded systems, which demand energy-efficient components. By lowering both static and dynamic power, multiplexer-based full adders help meet the stringent power requirements of these systems, extending battery life and reducing thermal output. The sustained performance improvements across area, speed, and power confirm that multiplexer-based full adders can effectively address the primary limitations of traditional multiplier designs, offering a viable alternative for achieving high performance with low hardware overhead.

However, while this design offers numerous benefits, additional optimization and testing are necessary to ensure compatibility with various digital applications and environmental conditions. Future research could explore scalability to larger bit-width multipliers and assess the robustness of the design under diverse voltage and temperature conditions.

Conclusion

This study demonstrates that multiplexer-based full adders provide an effective means of enhancing the compactness and performance of multiplier circuits. The proposed design achieves significant area savings, reduced delay, and lower power consumption compared to conventional multiplier architectures, underscoring its potential for use in high-speed, low-power applications. These improvements make the

International Journal of Advance Scientific Research
(ISSN – 2750-1396)
VOLUME 04 ISSUE 11 Pages: 1-5
OCLC – 1368736135

multiplexer-based multiplier architecture a valuable contribution to digital design, particularly in VLSI and embedded systems requiring optimized area and speed. Further investigation into larger-scale implementations and in-depth performance testing will be instrumental in establishing this design approach as a standard for efficient digital multipliers.

REFERENCE

1. C.Senthilpari, K.Diwakar and Ajay Kumar Singh "Low Power and High Speed 8x8 Bit Multiplier Using Nonclocked Pass Transistor Logics"November 2009
2. C.Senthilpari, K.Diwakar and Ajay Kumar Singh "High speed and High Throughput 8x8 Bit Multiplier using a Shannon –based Adder Cell"April 2009.
3. Padmanabhan Balasubramanian and Nikos E. Mastorakis "High Speed Gate Level Synchronous Full Adder Designs" WSEAS Transactions on circuits and systems February 2009
4. Z. Abid, H. El-Razouk, D.A. El-Dib "Low power multipliers based on new hybrid full adders" Microelectron. J (2008), doi:10.1016/ j.mejo.2008.04.002. International Journal of Embedded Systems and Applications (IJESA) Vol.2, No.2, June 2012 16
5. Donald A. Neamen "Microelectronics: Circuit Analysis and Design" third international edition, ISBN 007-125443-9, 2007, pp.137-139.
6. Zhijun Huang, "High level optimization techniques for low power multiplier design" 2003
7. D. Markovic, B. Nikolic and V.G. Oklobdzija "A general method in synthesis of pass-transistor circuits" Microelectronics Journal31, 2000, pp.991–998.
8. Reto Zimmermann and Wolfgang Fichtner "Low-Power Logic Styles: CMOS versus Pass-Transistor Logic" IEEE Journal of Solid-State Circuits, Vol.32, No.7, April 1997, pp.1079–1090.
9. C.Senthilpari, K.Diwakar, Ajay Kumar Singh, S.Kavitha, A.Arokiasamy "An Efficient 16-bit Non- Clocked Pass gates Adder Circuit with Improved Power Performance on Power Constraint.