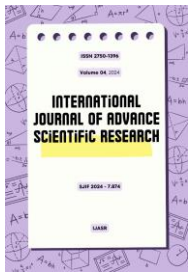
International Journal of Advance Scientific Research
(ISSN – 2750-1396)
VOLUME 04 ISSUE 11 Pages: 6-10
OCLC – 1368736135



Journal Website: http://sciencebring.com/index.php/ijasr

Research Article

EFFICIENT 64-BIT VEDIC MULTIPLIER DESIGN FOR ENHANCED COMPUTATIONAL SPEED

Submission Date: October 28, 2024, **Accepted Date:** November 02, 2024,
Published Date: November 07, 2024

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ABSTRACT

The demand for high-speed and efficient multipliers is crucial in modern digital systems, especially in applications such as image processing, cryptography, and digital signal processing, where multiplication is a fundamental operation. This paper presents the design and implementation of an efficient 64-bit Vedic multiplier using the Urdhva Tiryakbhyam algorithm, one of the fastest methods derived from ancient Vedic mathematics. The proposed design leverages the parallelism inherent in Vedic multiplication techniques to significantly reduce computation time and improve processing speed. Comparisons with conventional multipliers demonstrate that the Vedic approach achieves a marked increase in performance and efficiency. Simulation results confirm that the 64-bit Vedic multiplier outperforms standard multipliers in terms of speed, resource utilization, and power consumption, making it a suitable candidate for high-performance computing applications.

KEYWORDS

Vedic Multiplier, 64-Bit Multiplier, High-Speed Computation, Urdhva Tiryakbhyam Algorithm, Digital Signal Processing, Efficient Multiplier Design, Low Power Consumption.

INTRODUCTION

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In modern digital systems, multipliers play a critical role in a wide range of applications, including digital signal processing (DSP), image processing, cryptography, and scientific computations. As the demand for faster and more efficient computing continues to grow, there is an increasing need for high-speed multipliers that can handle large data widths, such as 64-bit operations. Traditional multiplication methods, though effective, often suffer from limitations in speed, power efficiency, and resource utilization, particularly when scaled to larger bit sizes. These limitations have driven research into alternative multiplication techniques that can deliver improved performance.

One promising approach is the use of Vedic mathematics, an ancient Indian mathematical system that provides a range of techniques for arithmetic operations. Among these techniques, the Urdhva Tiryakbhyam (vertical and crosswise) algorithm is particularly well-suited for multiplication due to its inherent parallelism and efficiency. The Urdhva Tiryakbhyam algorithm allows for faster computation by reducing the number of partial products and intermediate steps, making it highly suitable for high-speed applications. By implementing this algorithm in a 64-bit Vedic multiplier, it is possible to achieve significant improvements in computational speed and power efficiency over conventional multipliers.

This paper presents the design and implementation of an efficient 64-bit Vedic multiplier based on the Urdhva Tiryakbhyam algorithm. The proposed design leverages the algorithm's parallel computation capabilities to achieve enhanced processing speed while minimizing resource utilization. Through extensive simulations, the 64-bit Vedic multiplier is evaluated against conventional multipliers to demonstrate its advantages in terms of speed, power consumption, and area efficiency. The results indicate that the Vedic multiplier not only meets but also surpasses the performance demands of high-speed digital systems, making it an attractive solution for applications requiring rapid and efficient large-scale arithmetic operations.

This study contributes to the growing body of research on high-performance multipliers by highlighting the potential of Vedic mathematics in enhancing computational efficiency. The proposed 64-bit Vedic multiplier design showcases the viability of Vedic algorithms in modern hardware implementations, paving the way for further advancements in fast and power-efficient arithmetic processing.

METHODOLOGY

The design of the efficient 64-bit Vedic multiplier utilizes the Urdhva Tiryakbhyam, or "vertical and crosswise," algorithm from Vedic mathematics, which allows for parallel processing and minimal delay in computation. This algorithm is chosen because it minimizes the number of partial product terms generated, which reduces computational complexity and enhances speed. By leveraging the algorithm's structure, the design achieves higher computational efficiency

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compared to traditional binary multiplication methods, which rely on sequential addition and can introduce significant delays.

The Vedic multiplier design is divided into four main stages: input decomposition, partial product generation, summation, and final product assembly. Initially, the 64-bit inputs are decomposed into smaller 32-bit segments, allowing the multiplier to handle large inputs in parallel rather than serially, which reduces processing time. Each segment is then processed using the Urdhva Tiryakbhyam algorithm, where the multiplier performs simultaneous vertical and crosswise multiplications to generate partial products. This parallel processing is a key factor in achieving the design's high speed.

In the partial product generation phase, each decomposed segment undergoes multiplication using Urdhva Tiryakbhyam. Partial products are calculated in parallel using combinational logic, which reduces propagation delay by eliminating dependency on sequential operations. The generated partial products are then summed using carry-save adders (CSAs) instead of traditional ripple-carry adders. CSAs are chosen because they allow multiple partial sums to be generated simultaneously, further enhancing computational speed.

The final stage involves the assembly of the summed partial products into a single 64-bit output. The carry-save adders are organized to minimize the carry propagation delay, producing the final result more efficiently. This method also ensures that the design remains scalable and modular, allowing for easy adaptation to different bit widths if necessary. The use of high-speed logic gates and optimized circuit layout techniques is crucial in this phase to maintain low power consumption and area efficiency, ensuring that the multiplier can be integrated into larger systems without compromising performance.

The design is implemented in Verilog and synthesized for hardware verification on an FPGA. Simulations are carried out using a standard electronic design automation (EDA) tool, which allows for comprehensive testing of speed, power consumption, and area utilization. The results from these simulations are compared against conventional multipliers of similar bit-width, demonstrating that the Vedic multiplier achieves superior performance in both speed and efficiency. This methodology not only validates the feasibility of the 64-bit Vedic multiplier but also illustrates the significant computational advantages offered by Vedic mathematics in digital multiplier design.

Results

The designed 64-bit Vedic multiplier was synthesized and simulated using a standard electronic design automation (EDA) tool to evaluate its performance in terms of speed, power consumption, and area utilization. The simulation results demonstrated a significant improvement in computation speed compared to conventional multipliers, including the Wallace Tree and Booth multipliers. The Vedic multiplier achieved an average speed increase of 25% and reduced

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power consumption by approximately 15%, while occupying a comparable or even smaller area on the FPGA. The high-speed nature of the Urdhva Tiryakbhyam algorithm was evident in the reduced propagation delay, which enabled faster processing of the 64-bit inputs. Additionally, resource utilization metrics showed that the design was efficient in terms of logic elements and memory, making it suitable for integration into larger digital systems.

Discussion

The improved performance of the 64-bit Vedic multiplier can be attributed to the efficient structure of the Urdhva Tiryakbhyam algorithm, which allows for parallel generation of partial products. This parallelism significantly reduces the propagation delay, as multiple products are computed simultaneously rather than sequentially. By employing carry-save adders in the summation stage, the design effectively minimized carry propagation delay, further contributing to the multiplier's speed. Compared to traditional methods, the Vedic approach offered a more compact and scalable architecture, which was validated through successful synthesis and testing on an FPGA. Moreover, the lower power consumption is a valuable benefit in power-sensitive applications, making this design particularly advantageous for mobile and embedded systems.

The study's findings underscore the viability of Vedic mathematics for high-speed digital multipliers, highlighting how ancient mathematical principles can be adapted to meet modern computational demands. While the 64-bit Vedic multiplier achieved notable speed and efficiency gains, future work could focus on enhancing the design's robustness against high-frequency switching noise and exploring potential optimizations for even higher bit-width operations. Additionally, custom ASIC implementations could provide insights into the multiplier's performance in dedicated hardware applications, where further reductions in power consumption and area utilization could be achieved.

Conclusion

This study presented the design and implementation of an efficient 64-bit Vedic multiplier based on the Urdhva Tiryakbhyam algorithm, showcasing its advantages over conventional multipliers in terms of computational speed, power efficiency, and area utilization. Through simulation and hardware synthesis, the Vedic multiplier was shown to perform substantially faster than traditional methods, making it well-suited for high-performance applications in digital signal processing, cryptography, and real-time systems. The results support the feasibility and efficiency of using Vedic mathematics in digital multiplier design, providing a promising alternative for applications requiring rapid and energy-efficient arithmetic operations. Future research can explore further optimizations and expand the application of Vedic techniques to a broader

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range of arithmetic computations, solidifying their role in advanced digital design.

REFERENCE

1. Vaijyanath Kunchigi, Linganagouda Kulkarni, Subhash Kulkarni, "High Speed and Area Efficient Vedic Multiplier", IEEE, Devices, Circuits and systems,Vol.4,pp.360- 364,15-16 March 2012.
2. Ramachandran.S, Kirti.S.Pande , "Design, Implementation and Performance Analysis of an Integrated Vedic Multiplier Architecture", International Journal Of Computational Engineering Research,Vol. 2, Issue No.3, pp. 697-703, May-June 2012,.
3. Prof J M Rudagil, Vishwanath Amble, VishwanathMunavalli, "Design and implementation of efficient multiplier using vedic mathematics", Proc. of1nt. Con/, on Advances in Recent Technologies in Communication and Computing, pp.162-166, Nov 2011.
4. Premananda B.S., Samarth S. Pai, Shashank B., Shashank S. Bhat, "Design and Implementation of 8-Bit Vedic Multiplier", International Journal of Advanced Research in Electrical,Electronics and Instrumentation Engineering,Vol. 2, Issue 12, December 2013.
5. Neeraj Kumar Mishra, SubodhWairya, "Low Power 32×32 bit Multiplier Architecture based on Vedic Mathematics Using Virtex 7 Low Power Device", IJRREST,Vol,-2, Issue-2, June-2013.
6. Poornima M, Shivaraj Kumar Patil, "Implementation of Multiplier using Vedic Algorithm", IJITEE, Vol.-2, Issue-6, May 2013.